

What is claimed is:

- 1 1. A test unit comprising:  
2 an air source to generate a substantially constant temperature air stream;  
3 a test fixture to hold a die; and  
4 an enclosure for substantially surrounding the test fixture, the enclosure in  
5 operative communication with the air source, the enclosure constructed and arranged for  
6 coupling the temperature controlled air stream from the air source to the test fixture, and  
7 the enclosure including a non-conductive core comprising a plurality of surfaces, wherein  
8 one or more of the plurality of surfaces comprises a conductive coating applied to at least  
9 a portion thereof and at least one of the plurality of surfaces contacting the test fixture  
10 comprises a substantially uncoated surface.
- 1 2. The test unit of claim 1, wherein the non-conductive core comprises fiberglass.
- 1 3. The test unit of claim 1, wherein the conductive coating comprises a  
2 semiconductor.
- 1 4. The test unit of claim 1, wherein the conductive coating comprises a metal.
- 1 5. The test unit of claim 4, wherein the metal comprises aluminum.
- 1 6. The test unit of claim 1, wherein at least one of the plurality of surfaces has a  
2 connector.
- 1 7. The test unit of claim 6, wherein the connector comprises a snap-on ground  
2 connector.
- 1 8. The test unit of claim 1, wherein the uncoated surface has a plurality of locating  
2 holes.

1 9. The test unit of claim 8, wherein the test fixture has a plurality of locating pins  
2 and wherein each of the plurality of locating pins is capable of being inserted into at least  
3 one of the plurality of locating holes.

1 10. The test unit of claim 1, wherein the enclosure has one or more vent holes.

1 11. The test unit of claim 10, wherein the enclosure has a first end and a second end  
2 and each of the one or more vent holes is located about half way between the first end and  
3 the second end.

1 12. The test unit of claim 1, wherein the uncoated surface includes at least one  
2 substantially chamfered edge.

1 13. The test unit of claim 12, wherein the at least one substantially chamfered edge is  
2 uncoated.

1 14. A method of preparing a die for testing, the method comprising:  
2 inserting a die in a test fixture having a base;  
3 surrounding the test fixture with an enclosure in operative communication with a  
4 substantially constant temperature air stream, the enclosure having one or more exposed  
5 surfaces, each of the one or more exposed surfaces being a conductive surface;  
6 coupling each of the one or more exposed surfaces to a source of reference  
7 potential; and  
8 allowing the substantially constant temperature air stream to flow through the  
9 enclosure and over the die.

1 15. The method of claim 14, wherein forcing the substantially constant temperature  
2 air stream through the enclosure comprises:  
3 injecting an ionized air stream through the enclosure.

1 16. The method of claim 14, further comprising:  
2 attaching the enclosure to the test fixture; and  
3 forming a substantially air tight coupling between the enclosure and the source of  
4 the substantially constant temperature air stream.

1 17. An enclosure comprising:  
2 a hollow substantially cylindrical insulating core having a first orifice having a  
3 first diameter and at least one further orifice, the first orifice constructed and arranged for  
4 coupling the interior of the insulating core to a temperature controlled air source and a  
5 second orifice constructed and arranged for allowing air entering the core through the first  
6 orifice to pass over a test fixture substantially enclosed within the core prior to exiting  
7 through the further orifice, the hollow substantially cylindrical insulating core being  
8 partially coated with a conductive material maintained at a reference potential relative to  
9 the test fixture.

1 18. The enclosure of claim 17, wherein the hollow substantially cylindrical insulating  
2 core comprises fiberglass.

1 19. The enclosure of claim 17, wherein the first diameter is about 4.5 inches.

1 20. The enclosure of claim 17, wherein the conductive material comprises a  
2 semiconductor.

1 21. The enclosure of claim 17, wherein the conductive material comprises a metal.

1 22. The enclosure of claim 21, wherein the metal comprises copper.

1 23. The enclosure of claim 17, wherein the enclosure has at least two uncoated  
2 chamfered edges.

1 24. A method of fabricating an enclosure, the method comprising:  
2 forming a cylindrically shaped block of insulating material having a substantially  
3 flat first end, a substantially flat second end, and an outer surface;  
4 forming a first hole having a first diameter in the cylindrically shaped block to  
5 form a first inner surface;  
6 forming a second hole having a second diameter in the cylindrically shaped block  
7 to form a second inner surface, the second diameter being greater than the first diameter;  
8 and  
9 coating the outer surface, the substantially flat first end, the first inner surface, and  
10 the second inner surface with a conductive material.

1 25. The method of claim 24, wherein coating the outer surface, the first end, the first  
2 inner surface, and the second inner surface with a conductive material comprises:  
3 coating the outer surface, the first end, the first inner surface and the second inner  
4 surface with aluminum.

1 26. The method of claim 25, wherein coating the outer surface, the first end, the first  
2 inner surface and the second inner surface with aluminum comprises:  
3 depositing the aluminum on the outer surface, the first end, the first inner surface  
4 and the second inner surface by chemical vapor deposition.

1 27. The method of claim 24, wherein coating the outer surface, the first end, the first  
2 inner surface, and the second inner surface with a conductive material comprises:  
3 coating the outer surface, the first end, the first inner surface and the second inner  
4 surface with a semiconductor.

1 28. The method of claim 27, wherein coating the outer surface, the first end, the first  
2 inner surface and the second inner surface with a semiconductor comprises:

3 painting the semiconductor on the outer surface, the first end, the first inner  
4 surface and the second inner surface.

1 29. The method of claim 27, wherein coating the outer surface, the first end, the first  
2 inner surface and the second inner surface with a semiconductor comprises:  
3 spraying the semiconductor on the outer surface, the first end, the first inner  
4 surface and the second inner surface.